CLAIMS

1. A method for forming a transistor, the method comprising the steps of:

a) providing a semiconductor substrate;

b) patterning the semiconductor substrate to provide a first body edge;

c) providing a first gate structure of a first fermi level adjacent said first body edge;

d) patterning the semiconductor substrate to provide a second body edge, the first and second body edges of the semiconductor substrate defining a transistor body; and

e) providing a second gate structure of a second fermi level adjacent said second body edge.

2. The method of claim 1 wherein the first gate structure of a first fermi level comprises p-type material and wherein the second gate structure of a second fermi level comprises n-type material.

3. The method of claim 1 wherein the first gate structure of a first fermi level comprises n-type material and wherein the second gate structure of a second fermi level comprises p-type material.

4. The method of claim 1 wherein the semiconductor substrate comprises a silicon-on-insulator layer, and wherein the step of patterning the semiconductor substrate to provide a first body edge comprises patterning the silicon-on-insulator layer and wherein the step of patterning the semiconductor substrate to provide a second body edge comprises pattering the silicon-on-insulator layer.

5. The method of claim 1 further comprising the steps of forming a first gate dielectric layer on the first body edge and forming a second gate dielectric layer on the second body edge.

6. The method of claim 1 wherein the step of patterning the semiconductor substrate to provide a first body edge comprises forming a mandrel layer on the semiconductor substrate; patterning the mandrel layer to form an exposed side, and forming a sidewall spacer adjacent to the exposed side, and wherein a first edge of the sidewall spacer defines the first body edge.

7. The method of claim 6 wherein the step of patterning the semiconductor substrate to provide a second body edge comprises using a second edge of the sidewall spacer to define the second body edge.

8. The method of claim 1 further comprising the step of forming a source/drain implant into the body of the transistor by performing an angled implant into the transistor body.

9. The method of claim 1 further comprising the step of forming a substantially uniform dopant concentration density in the transistor body.

10. The method of claim 9 wherein the step of forming a substantially uniform dopant concentration density in the transistor body comprises performing a plurality of angled implants into the body.

11. The method of claim 1 wherein the of forming a substantially uniform dopant concentration density in the transistor body comprising forming a dopant concentration between 0.3 N_A and 3 N_A, where N_A is defined as:

$$N_A = \frac{2\varepsilon_{ox}Eg}{Toxs} \cdot \frac{(Toxs + \lambda)}{\left[(Toxs) + Toxw + Tsi \cdot \frac{\varepsilon_{ox}}{\varepsilon_{si}}\right]^2} \qquad \text{Eq. 2}$$

12. The method of claim 9 wherein the step of forming a substantially uniform dopant concentration density in the transistor body comprises performing a first angled implant when the first body edge is exposed and performing a second angled implant when the second body edge is exposed.

13. The method of claim 11 wherein the first angled implant comprises an implant at approximately 45° with respect to the semiconductor substrate and wherein the second angled implant comprises an implant at approximately 45° with respect to the semiconductor substrate.

14. The method of claim 1 wherein the step of patterning the semiconductor substrate to provide a first body edge comprises forming a mandrel layer on the semiconductor substrate; patterning the mandrel layer, and using the patterned mandrel layer to define the first body edge.

15. The method of claim 14 wherein the step of patterning the semiconductor substrate to provide a second body edge comprises forming a sidewall spacer adjacent to a gate material layer and using the sidewall spacer to define the second body edge.

16. A method for forming a field effect transistor, the method comprising the steps of:

a) providing a silicon-on-insulator substrate, the silicon-on-insulator substrate comprising a silicon layer on a buried dielectric layer;

b) forming a mandrel layer on the silicon layer; patterning the mandrel layer to define a mandrel layer edge;

c) patterning the silicon layer with the mandrel layer edge the patterning of the silicon layer providing a first body edge;

d) forming a first gate dielectric on the first body edge;

e) providing a first gate structure of a first fermi level adjacent the first body edge on the first gate dielectric;

f) patterning the mandrel layer to expose a first edge of the first gate structure;

g) forming a sidewall spacer adjacent the first edge of the first gate structue, the sidewall spacer having a first edge and a second edge;

h) patterning the silicon layer with the second edge of the sidewall spacer, the pattering of the silicon layer providing a second body edge, where the first and second body edges of the patterned silicon layer define a transistor body;

i) providing a second gate dielectric on the second body edge; and

j) providing a second gate structure of a second fermi level adjacent the second body on the second gate dielectric.

17. The method of claim 16 wherein the first gate structure of a first fermi level comprises p-type polysilicon material and wherein the second gate structure of a second fermi level comprises n-type polysilicon material.

18. The method of claim 16 wherein the first gate structure of a first fermi level comprises n-type polysilicon material and wherein the second gate structure of a second fermi level comprises p-type polysilicon material.

19. The method of claim 16 further comprising the step of forming a source/drain implant into the body of the transistor by performing an angled implant into the transistor body.

20. The method of claim 16 wherein the step of depositing sidewall spacer material in sidewall spacer trough comprises forming a sidewall oxide layer in said trough, forming a nitride layer over said sidewall oxide layer, and filling said sidewall spacer trough with a deposition of oxide.

21. The method of claim 16 further comprising the step of forming a substantially uniform dopant concentration density in the transistor body.

22. The method of claim 21 wherein the step of forming a substantially uniform dopant concentration density in the transistor body comprises performing a plurality of angled implants into the body.

23. The method of claim 21 wherein the step of forming a substantially uniform dopant concentration density in the transistor body comprises performing a first angled implant when the first body edge is exposed and performing a second angled implant when the second body edge is exposed.

24. The method of claim 23 wherein the first angled implant comprises an implant at approximately 45° with respect to the silicon-on-insulator substrate and wherein the second angled implant comprises an implant at approximately 45° with respect to the silicon-on-insulator substrate.

25. A transistor comprising:

a) a transistor body formed on a substrate, the transistor body having a first vertical edge and a second vertical edge;

b) a first gate structure adjacent the transistor body first vertical edge, the first gate structure having a first fermi level; and

c) a second gate structure adjacent the transistor body second vertical edge, the second gate structure having a second fermi level.

26. The transistor of claim 25 wherein the first gate structure comprises p-type material and wherein the second gate structure comprises n-type material.

27. The transistor of claim 25 wherein the first gate structure comprises n-type material and wherein the second gate structure comprises p-type material.

28. The transistor of claim 25 wherein the transistor body comprises a portion of a silicon-on-insulator layer.

29. The transistor of claim 25 wherein the first and second gate structures comprise polysilicon.

30. The transistor of claim 25 further comprising a first gate dielectric between the transistor body first edge and the first gate structure and a second gate dielectric between the transistor body second edge and the second gate structure.

31. The transistor of claim 25 wherein the transistor body comprises a source/drain implant into the transistor body.

32. The transistor of claim 25 wherein the transistor body has a substantially uniform dopant concentration density.

33. The transistor of claim 32 wherein the substantially uniform dopant concentration density is comprises a plurality of angled implants into the transistor selected to result in a substantially uniform dopant concentration density.

36. A double gated field effect transistor comprising:

a) a transistor body, the transistor body formed from a silicon layer formed above an insulator layer , the transistor body having a first vertical edge and a vertical second edge, wherein the transistor body first edge and the transistor body second edge are opposite each other and substantially perpendicular to the insulator layer;

b) a first gate dielectric layer formed on the transistor body first edge;

c) a second gate dielectric layer formed on the transistor body second edge;

d) a first gate structure formed on the first gate dielectric layer adjacent to the transistor body first edge, the first gate structure comprising p-type polysilicon; and

e) a second gate structure formed on the second gate dielectric layer adjacent to the transistor body second edge, the second gate structure comprising n-type polysilicon.

37. The double gated field effect transistor of claim 36 further comprising a source/drain implant in the transistor body formed by performing an angled implant into the transistor body.

38. The double gated field effect transistor of claim 36 wherein the body comprises a substantially uniform dopant concentration density.

34. The transistor of claim 32 wherein the substantially uniform dopant concentration comprises a dopant concentration between 0.3 N_A and 3 N_A, where N_A is defined as:

$$N_A = \frac{2\varepsilon_{ox} Eg}{Toxs} \cdot \frac{(Toxs + \lambda)}{\left[(Toxs) + Toxw + Tsi \cdot \frac{\varepsilon_{ox}}{\varepsilon_{si}}\right]^2} \qquad \text{Eq. 2}$$

35. The transistor of claim 25 wherein the transistor body first edge is opposite the transistor body second edge and wherein the transistor body first edge and transistor body second edge are substantially perpendicular to a top surface of the substrate.

39. The double gated field effect transistor of claim 38 wherein the substantially uniform dopant concentration density is formed by performing a plurality of angled implants into the transistor body.

40. The double gated field effect transistor of claim 36 further comprising a polysilicon plug to electrically couple the first gate structure to the second gate structure.

41. A method for forming a semiconductor device, the method comprising the steps of:

a) forming a single crystal semiconductor fin having a first side and a second side;

b) tilt implanting said first side of the single crystal semiconductor fin and tilt implanting said second side of the single crystal semiconductor fin.

42. The method of claim 41 wherein the step of forming a single crystal semiconductor fin comprises patterning a silicon on insulator layer to define a transistor body.

43. The method of claim 41 further comprising the step of providing a first gate structure of a first fermi level adjacent said first said and providing a providing a second gate structure of a fermi level function adjacent said second side.

44. The method of claim 43 wherein the first gate structure of a first fermi level comprises p-type material and wherein the second gate structure of a second fermi level comprises n-type material.

45. The method of claim 43 further comprising the steps of forming a first gate dielectric layer on the first side and forming a second gate dielectric layer on the second side.

46. The method of claim 41 wherein the step of forming the single crystal semiconductor fin comprises forming a mandrel layer on a semiconductor layer; patterning the mandrel layer to form an exposed side, wherein the exposed side of the mandrel layer defines the first side of the single crystal semiconductor fin.

47. The method of claim 46 wherein the step of forming the single crystal semiconductor fin further comprises forming a sidewall spacer, the sidewall spacer defining the second side of the single crystal semiconductor fin.

48. The method of claim 41 wherein the step of tilt implanting the first side and tilt implanting the second side provide a substantially uniform dopant concentration density in the single crystal semiconductor fin.

49. The method of claim 48 wherein the of forming a substantially uniform dopant concentration density in the transistor body comprising forming a dopant concentration between 0.3 N_A and 3 N_A, where N_A is defined as:

$$N_A = \frac{2\varepsilon_{ox}Eg}{Toxs} \cdot \frac{(Toxs + \lambda)}{\left[(Toxs) + Toxw + Tsi \cdot \frac{\varepsilon_{ox}}{\varepsilon_{si}}\right]^2} \qquad \text{Eq. 2}$$

50. The method of claim 41 wherein the step of tilt implanting said first side of the single crystal semiconductor fin and tilt implanting said second side of the single crystal semiconductor fin comprises implanting at approximately 45° with respect to the first side and at approximately 45° with respect to the second side.

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